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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of _____ : January 30, 2004
Daniel C. Edelstein, et al. : Group Art Unit:
Serial No. 10/707,713 : Examiner: to be assigned
Filed: 1/6/04 : International Business Machines Corporation
2070 Route 52
Hopewell Junction, NY 12533

TITLE: COMPLIANT PASSIVATED EDGE SEAL FOR LOW-K INTERCONNECT STRUCTURES

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

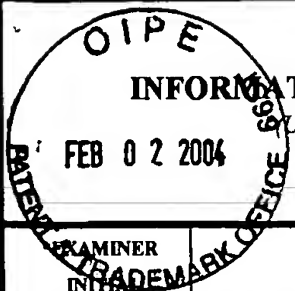
Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,
Daniel C. Edelstein, et al.

By Margaret A. Pepper
Margaret A. Pepper
Registration No. 45,008
Telephone No. 845-894-4713

 <p>INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)</p>		Docket Number (Optional) FIS920030255US1		Application Number 10/707,713	
		Applicant(s) Daniel C. Edelstein, et al.			
		Filing Date 1/6/04		Group Art Unit Not Yet Assigned	
EXAMINER INITIALS		OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)			
		H. A. Reed et al., "Compliant Wafer Level Package (CWLP) With Embedded Air-Gaps For Sea of Leads (SoL) Interconnections," Proc. of IEEE 2001 International Interconnect Technology Conference, pp. 151-153.			
		M.S. Bakir et al., "Sea of Leads Microwave Characterization and Process Integration with FEOL and BEOL," Proc. of IEEE 2002 International Interconnect Technology Conference, pp. 116-118.			
		A. Mule et al., "Optical Waveguides With Embedded Air-Gap Cladding Integrated Within a Sea-of-Leads (SoL) Wafer-Level Package," Proc. of IEEE 2002 International Interconnect Technology Conference, pp. 122-124.			
		"Chip Pad Process" IBM Technical Disclosure bulletin, Oct. 1991.			
		"Via Reliability Problem Eliminated by an Offset Elliptical Via," IBM Technical Disclosure Bulletin, Jan. 1998, pp. 310-311			
		"Structure for the Passivation of Semiconductor Chips," IBM Technical Disclosure Bulletin, Aug. 1973, p. 728			
EXAMINER		DATE CONSIDERED			
<p>*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>					